High-Frequency Flexible Graphene Field-Effect Transistors with Short Gate Length of 50 nm and Record Extrinsic Cut-Off Frequency

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Flexible graphene field effect transistors (GFETs) are fabricated on a polyimide (PI) substrate by an improved self-aligned fabrication procedure. Short gate length of 50 nm is achieved. Ohmic contact resistance is depressed. The prepared GFET shows comparable intrinsic cut-off frequency and maximum oscillation frequency of 116 and 110 GHz, respectively. The high frequency of flexible GFET demonstrated here paves the way for applications which require high flexibility and radio frequency operations.

Graphene field effect transistors (GFETs) have great application potential in the next generation flexible electronics due to its exceptional electronic properties (room temperature mobility of 200 000 $cm^2 V^{-1} s^{-1}$, and saturation velocity of 5×10^7 $cm\,s^{-1}$), and outstanding mechanical performance (strain limits up to 25%).[1–5] Large area graphene films can be produced in commercially scalable processes by chemical vapor deposition (CVD) on copper foils and can be transferred to any target substrate.[6]

GFETs with intrinsic cut-off frequency (f_T) of 427 GHz[7] and maximum oscillation frequency (f_{max}) of 220 GHz have been demonstrated on a rigid substrate.[8] For flexible GFETs, the cut-off frequency reached 198 GHz[9] and the maximum oscillation frequency reached 34 GHz,[10] respectively, which fall far short of that of a GFET on a rigid substrate. To further improve the performance of flexible GFETs, some limited parameters including high parasitic parameters (parasitic resistance arising from the ungated channel regions and the metal-graphene Ohmic contacts), and high interfacial defect density at the metal/dielectric/graphene stacks should be suppressed further. Channel lengths scaling is another reason for their limited performances.

In this work, we fabricate flexible FETs with CVD graphene as the active channel material with a 50-nm channel length by an improved self-aligned process. The devices demonstrate extrinsic f_T and f_{max} up to 56 and 14.5 GHz, intrinsic f_T and f_{max} up to 116 and 110 GHz, respectively.

Experimental Details: Graphene used for device fabrication was grown by low pressure CVD technique on Cu foil, followed by a wet transfer process onto a polyimide (PI) substrate. The GFETs are fabricated by an improved self-aligned fabrication procedure following our previously published method.[11] A 20-nm thick Au metal film was deposited on the surface of the transferred graphene on PI substrate by e-beam evaporation under an ultra high vacuum. The channel regions was defined by optical lithography. After removal of the Au film outside the channel by wet etch of Au by KI:I_2 solution, the electrical isolation was realized by exposing the graphene to oxygen plasma. Rectangular gates of 50 nm were patterned by electron-beam lithography. Subsequently, the Au layer under the gates was wet-etched to form a self-aligned source and drain Ohmic contacts, automatically. Two-nanometer thick Al was deposited by e-beam evaporation, and then oxidized in air for 1 day at room temperature to form an AlO_x dielectric. The self-oxidized AlO_x dielectric layer is of good quality and exhibits excellent insulation with negligible gate leakage current of around 4 pA (with $-2\,V \le V_{gs} \le 2\,V$, gate length $L_g = 50$ nm, gate width $W_g = 8\,\mu m$, and gate leakage current density 1 $mA\,cm^{-2}$). Finally, a 100-nm-thick Al metal film was evaporated to form the gate electrodes.

Results and Discussion: **Figure 1** shows the SEM images of a dual rectangular gate GFET with gate width of 8 $\mu m \times 2$. It can be seen that the gate length is ≈50 nm, and the wet-etched source and drain space is ≈1 μm.

Figure 2 shows the DC characteristics of GFET with strain increasing from $\varepsilon = 0$–1.5%. The strain is uniaxial tensile strains. The sketch map of bending of the GFET is shown in the inset of Figure 2(b). The bending induced tensile strain is calculated through the curvature radius in a form given by $\varepsilon = t/(2r + t)$, where $t = 250\,\mu m$ is the thickness of the substrate and r is the bending radius. The DC electrical transport measurements were conducted using a Semiconductor Parameter Analyzer (SPA). The GFET shows p-type doping with the Dirac point at a gate

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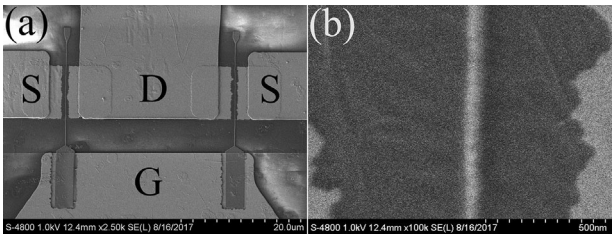


Figure 1. SEM images of a dual rectangular gate GFET with gate length of 50 nm and gate width of 8 μm × 2. a) The GFET and b) magnification of the gate electrode.

voltage of $V_{Dirac} > 1$ V. At $\varepsilon = 0$, the maximum scaled on-current I_{ds} reached 0.57 A mm^{-1} at $V_{ds} = -0.5$ V and $V_{gs} = -1$ V, as shown in Figure 2(a). The total on-resistance can be derived from the current–voltage characteristics shown in Figure 2(a) by $R_{total} = dV_{ds}/dI_{ds}$ at low V_{ds}. The total resistance is composed of the access resistance of the ungated graphene channel, graphene channel resistance, and contact resistance of the source/drain metal to graphene channel, and $R_{total} = R_{access} + R_{channel} + 2R_c$. The contact resistances R_c can be estimated by $R_c = (R_{total} - R_{access})/2$. $R_{total} = 650\,\Omega \cdot \mu m$. The sheet resistance of the graphene is around $R_s = 400\,\Omega$/square. $R_{access} = R_s \times L_{access} = 400\,\Omega \cdot \mu m$. The derived contact resistance R_c is 125 Ω · μm, indicating good Ohmic contact.

With strain increasing from $\varepsilon = 0$–1.5%, the maximum scaled on-current I_{ds} gradually decreases to 0.4 A mm^{-1}. Figure 2(d) shows the transfer characteristics of GFET under different strain.

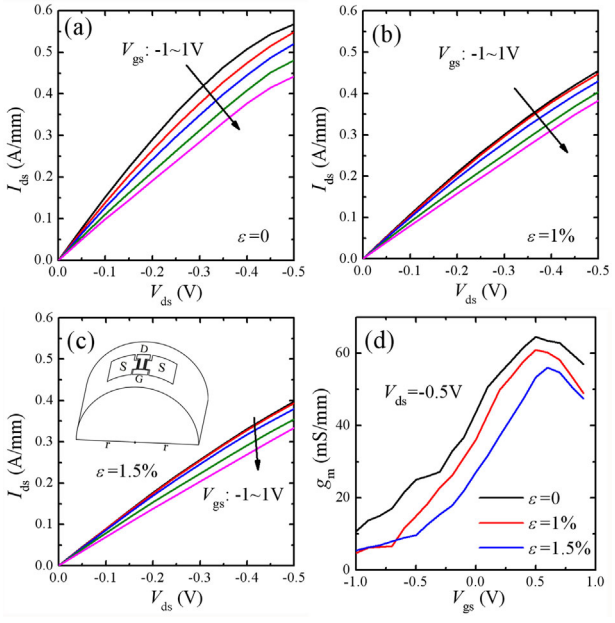


Figure 2. The DC characteristics of GFET with gate length of 50 nm and gate width of 8 μm × 2 under different tensile strains. Current–voltage characteristics of GFET under (a) $\varepsilon = 0$, (b) $\varepsilon = 1\%$, and (c) $\varepsilon = 1.5\%$. The I_{ds}–V_{ds} curves are measured at gate voltage ranging from −1 to 1 V in 0.5 V increments. d) Transfer characteristics of GFET at $V_{ds} = -0.5$ V with $-1\,V \le V_{gs} \le 1$ V. The inset in (c) shows the sketch map of bending of the GFET.

The maximum transconductance (g_m) is 65 mS mm^{-1} and decreases slightly with strain.

The main performance indexes of transistors for high-speed applications are the cutoff frequency f_T and maximum oscillation frequency f_{max}, which can be extracted from small-signal scattering (*S*) parameters. High-frequency *S* parameters measurements were carried out in the range of 1–30 GHz using a Vector Network Analyzer (VNA) with standard ground-signal-ground (GSG) probes. To calibrate the VAN and wafer-probing system, a standard substrate was used for short-open-load-through (SOLT) calibration procedure. To accurately evaluate the intrinsic transistor characteristics at RF frequencies, the customized open, and short test patterns on the PI substrate were designed for parasitic de-embedding. The open structure is identical in dimension and design to the transistor but does not include the graphene channel material.

Figure 3 shows the high-frequency characteristics of the GFET with gate length of 50 nm and gate width of 8 μm × 2. As shown in Figure 3(a), the extrinsic $f_{T\text{-}ext}$ reached 56 GHz for the GFET, which is the highest extrinsic f_T achieved in flexible graphene transistors reported to date.[9,10,12–16] The extrinsic $f_{max\text{-}ext}$ was 14.5 GHz for the GFET. Full de-embedding gave the intrinsic values of $f_{T\text{-}int} = 116$ GHz and $f_{max\text{-}int} = 110$ GHz. **Figure 4** shows the extrinsic and intrinsic f_T and f_{max} values under different tensile strains ($\varepsilon = 0$–2%). The extrinsic f_T and f_{max} exhibit 46% and 39% degradation, and the intrinsic f_T and f_{max} exhibit 53% and 54% degradation, respectively.

Figure 5 shows the comparisons of extrinsic and intrinsic f_T of our flexible GFET with published data[9,10,13,17] and their dependence on gate length. The extrinsic and intrinsic f_T values of our flexible GFET show good consistent with the scaling trend of $f_T \propto 1/L_g$. Channel length scaling is an important reason for the increase in f_T and f_{max} from previously reported flexible GFETs. The improved self-aligned GFETs fabrication procedure is also helpful to the improvements of f_T and f_{max}. First, the graphene channel is photo-resist free and away from any undesired contamination during the whole fabrication. Second, the contact interface of the graphene channel with its Ohmic contact metal is kept clean, which can help to decrease the Ohmic contact resistance.[18]

The highest achievable current-gain cut-off frequency and maximum oscillation frequency in a FET are given by[12]

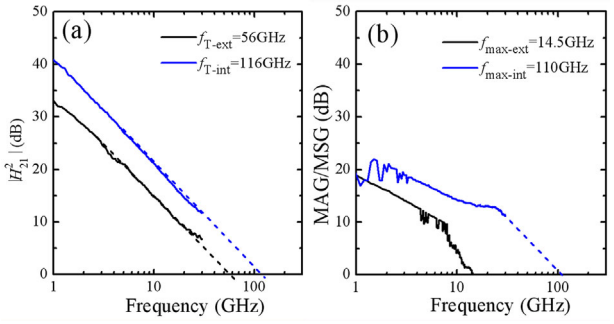


Figure 3. High-frequency characteristics of the GFET with gate length of 50 nm and gate width of 8 μm × 2. a) Measured and intrinsic $|H_{21}|^2$, and b) measured and intrinsic maximum stable/available gain (MSG/MAG) of the device.

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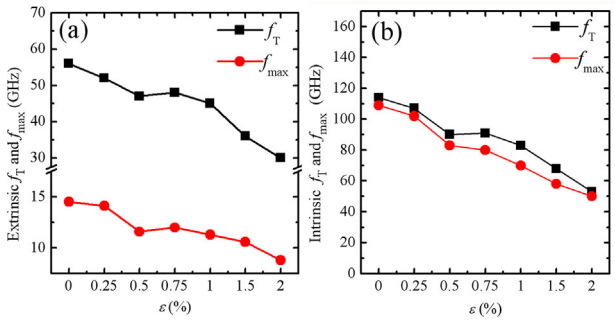


Figure 4. a) Extrinsic f_T and f_{max}, and b) intrinsic f_T and f_{max} of the GFET with gate length of 50 nm and gate width of 8 μm × 2 under different tensile strains of 0–2%.

$$f_{T-int} = g_m/2\pi(C_{gs} + C_{gd}) \quad (1)$$

$$f_{max-int} = f_{T-int}/2\sqrt{g_{ds}R_i} \quad (2)$$

The approximations for the extrinsic frequencies of the whole FET are

$$f_{T-ext} = f_{T-int}/1 + g_{ds}(R_s + R_d) + \frac{C_{gd}g_m(R_s + R_d)}{C_{gs} + C_{gd}} \quad (3)$$

$$f_{max-ext} = f_{T-int}/2\sqrt{g_{ds}(R_i + R_s + R_g) + g_m R_g \frac{C_{gd}}{C_{gs}}} \quad (4)$$

where C_{gs} and C_{gd} are gate-source capacitance and gate drain capacitance, respectively. g_m is the transconductance. g_{ds} is the drain conductance (the inverse of the drain differential resistance R_{ds}). R_i is the channel resistance. R_g is the gate pad resistance. R_s and R_d are the source/drain series resistances. **Table 1** shows the small signal model parameters of the GFET. The small signal equivalent circuit of the GFETs is shown in **Figure 6**. L_g, L_s, and L_d are gate/source/drain pad inductance. C_{pg}, C_{pgd}, and C_{pd} are parasitic gate pad capacitance, gate-drain parasitic capacitance, and drain parasitic capacitance, respectively. Our device show comparable intrinsic current-gain cut-off frequency $f_{T\text{-}int}$ and maximum oscillation frequency $f_{max\text{-}int}$. This is due to $2\sqrt{g_{ds}R_i} = 1.03$, which makes $f_{max\text{-}int}/f_{T\text{-}int}$ close to 1. The extrinsic $f_{max\text{-}ext}$ of 14.5 GHz is much lower than the extrinsic $f_{T\text{-}ext}$ of 56 GHz. This is mainly due to parasitism, especially the large gate parasitic resistance R_g, as shown by Eqs. (3) and (4). The 50-nm rectangular gates make the gate parasitic resistance R_g large. In the future, T-shape gate will be adopted to depress the gate resistance. Comparable extrinsic $f_{max\text{-}ext}$ and $f_{T\text{-}ext}$ are hopeful realization.

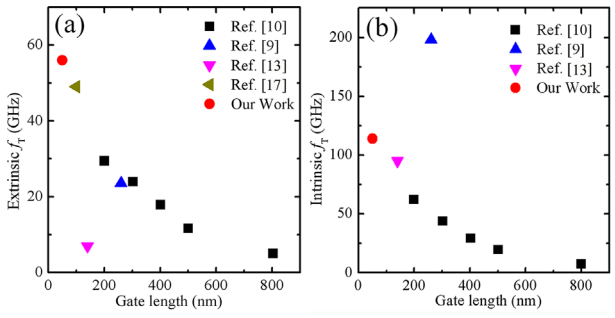


Figure 5. Scaling trend of the extrinsic and intrinsic f_T, and comparison to published data[9,10,13,17] for different gate-length flexible GFETs.

Table 1. Small signal model parameters of GFET with gate length of 50 nm and a gate width of 8 μm × 2.

C_{gs} (fF)	C_{gd} (fF)	g_{ds} (mS)	g_m (mS)	R_i (Ω)	R_g (Ω)	R_s (Ω)	R_d (Ω)
5.2	2.3	24	4.9	11	120	25	25

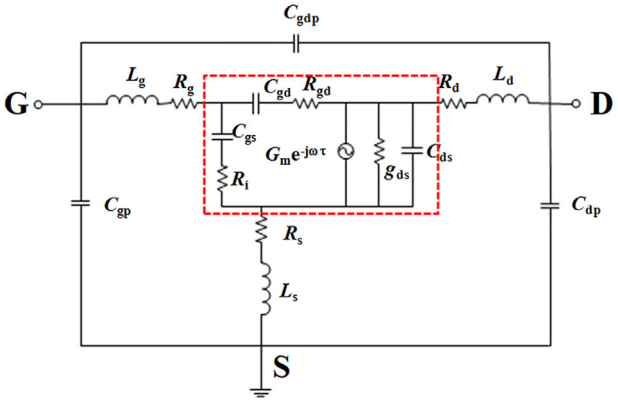


Figure 6. Small signal equivalent circuit of the GFET. The elements within the red rectangle constitute the intrinsic transistor.

In conclusion, flexible GFETs with very short gate-length of 50 nm were fabricated on a PI substrate. The GFET demonstrates an extrinsic f_T of 56 GHz, which is the highest extrinsic f_T achieved in flexible GFETs reported to date. The GFET also shows comparable intrinsic cut-off frequency and maximum oscillation frequency of 116 and 110 GHz, and still can work under strain up of 2%. Future improvements of device structures are essential to further improve the RF performance of flexible GFETs.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

cut-off frequency, flexible electronics, graphene, transistors

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